

FORM PTO-1449

LIST OF DOCUMENTS CITED BY APPLICANT

Atty. Docket No.

A-8753X

Serial No.

10/808 286

Applicant

Gerald J. BANKS

Filing Date

Herewith

03/25/04

Group

U. S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
Gu	AA	4,192,014	03/04/80	Craycraft	365	104	
	AB	4,357,685	11/02/82	Daniele et al.	365	189	
	AC	4,964,079	10/16/90	Devin	365	168	
	AD	5,172,338	12/15/92	Mehrotra et al.	365	185	
	AE	5,262,984	11/16/93	Noguchi et al.	365	185	
	AF	3,801,965	04/02/74	Keller et al.	340	173R	
	AG	4,004,159	01/18/77	Rai et al.	307	238	
	AH	4,054,864	10/18/77	Audaire et al.	340	173R	
	AI	4,090,258	05/16/78	Cricchi	365	184	
	AJ	4,122,541	10/24/78	Uchida	365	154	
Gu	AK	4,139,910	02/13/79	Anantha et al.	365	183	

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
Gu	AL	WO82/02276	07/08/82	WIPO	—	—	
	AM	WO82/02976	09/02/82	WIPO	—	—	
	AN	WO90/01984	03/08/90	WIPO	—	—	
	AO	2 630 574	10/27/89	France	—	—	Abstract
Gu	AP	0 390 404	10/03/90	Europe	—	—	
	AQ						

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Gu	AR	M. Bauer et al., A Multilevel-Cell 32Mb Flash Memory, 1995 IEEE International Solid-State Circuits Conference, Session 7, Paper TA7.7.					
Gu	AS	John A. Bayliss et al., The Interface Processor for the 32b Computer, 1981 IEEE International Solid-State Circuits Conference, February 1981, at 116-117.					

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94	AA*	4,149,270	04/10/79	Cricchi et al.	365	222	
	AB*	4,181,980	01/01/80	McCoy	365	45	
	AC*	4,272,830	06/09/81	Moench	365	45	
	AD*	4,287,570	09/01/81	Stark	365	104	
	AE*	4,300,210	11/10/81	Chakravarti et al.	365	45	
	AF*	4,306,300	12/15/81	Terman et al.	365	45	
	AG*	4,327,424	04/27/82	Wu	365	104	
	AH*	4,388,702	06/14/83	Sheppard	365	104	
	AI*	4,415,992	11/15/83	Adlhoch	365	94	
	AJ*	4,449,203	05/15/84	Adlhoch	365	104	
94	AK*	4,462,088	07/24/84	Giuliani et al.	365	105	

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
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OTHER (unclassified) citations: include date, document number, etc.

94	AR*	Christoph Bleiker & Hans Melchior, A Four-State EEPROM Using Floating-Gate Memory Cells, IEEE Journal of Solid-State Circuits, Vol. SC-22, No. 3, June 1987, at 260-263.					
94	AS*	Raymond A. Heald & David A. Hodges, Multilevel Random-Access Memory Using One Transistor Per Cell, IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 4, August 1976, at 519-528.					

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Ju	AA^	4,495,602	01/22/85	Sheppard	365	104	
	AB^	4,503,518	03/05/85	Iwahashi	365	104	
	AC^	4,558,241	12/10/85	Suzuki et al.	307	530	
	AD^	4,578,777	03/25/86	Fang et al.	365	184	
	AE^	4,586,163	04/29/86	Koike	365	104	
	AF^	4,627,027	12/02/86	Rai et al.	365	45	
	AG^	4,653,023	03/24/87	Suzuki et al.	365	104	
	AH^	4,661,929	04/28/87	Aoki et al.	365	189	
	AI^	4,709,350	11/24/87	Nakagome et al.	365	45	
	AJ^	4,733,394	03/22/88	Giebel	371	21	
Ju	AK^	4,771,404	09/13/88	Mano et al.	365	189	

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Ju	AR^	David A. Rich, A Survey of Multivalued Memories, IEEE Transactions on Computers, Vol. C-35, No. 2, February 1986, at 99-106.
Ju	AS^	R.S. Withers et al., Nonvolatile Analog Memory in MNOS Capacitors, IEEE Electron Device Letters, Vol. EDL-1, No. 3, March 1980, at 42-45.

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
ju	AA#	4,799,195	01/17/89	Iwahashi et al.	365	185	
	AB#	4,847,808	07/11/89	Kobatake	364	104	
	AC#	4,853,892	08/01/89	Hori	365	49	
	AD#	4,890,259	12/26/89	Simko	365	45	
	AE#	4,914,631	04/03/90	Johnson et al.	365	189.11	
	AF#	4,989,179	01/29/91	Simko	365	45	
	AG#	5,021,999	06/04/91	Kohda et al.	365	168	
	AH#	5,043,940	08/27/91	Harari	365	168	
	AI#	5,095,344	03/10/92	Harari	357	23.5	
	AJ#	5,163,021	11/10/92	Mehrotra et al.	365	185	
ju	AK#	5,258,958	11/02/93	Iwahashi et al.	365	210	

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
Qu	AA'	5,268,870	12/07/93	Harari	365	218	
	AB'	5,293,560	03/08/94	Harari	365	185	
	AC'	5,321,655	06/14/94	Iwahashi et al.	365	200	
	AD'	5,351,210	09/27/94	Saito	365	189.01	
	AE'	5,422,845	06/06/95	Ong	365	185	
	AF'	5,432,735	07/11/95	Parks et al.	365	168	
	AG'	5,434,825	07/18/95	Harari	365	185	
	AH'	5,440,505	08/08/95	Fazio et al.	365	45	
	AI'	5,444,656	08/22/95	Bauer et al.	365	189.01	
	AJ'	5,450,363	09/12/95	Christopherson et al.	365	205	
Qu	AK'	5,457,650	10/10/95	Sugiura et al.	365	184	

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Examiner Initial		Document Number	Date	Name	Class	Sub-class	Filing Date
Ju	AA~	5,469,384	11/21/95	Lacey	365	185.13	
	AB~	5,475,693	12/12/95	Christopherson et al.	371	10.2	
	AC~	5,485,422	01/16/96	Bauer et al.	365	168	
	AD~	5,497,119	03/05/96	Tedrow et al.	327	540	
	AE~	5,506,813	04/09/96	Mochizuki et al.	365	230.03	
	AF~	5,508,958	04/16/96	Fazio et al.	365	185.19	
	AG~	5,515,317	05/07/96	Wells et al.	395	427	
	AH~	5,523,972	06/04/96	Rashid et al.	365	185.22	
	AI~	5,539,690	07/23/96	Talreja et al.	365	185.22	
	AJ~	5,541,886	07/30/96	Hasbun	365	230.01	
Ju	AK~	5,544,118	08/06/96	Harari	365	218	

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Ju	AA❖	5,550,772	08/27/96	Gill	365	185.03	
	AB❖	5,568,439	10/22/96	Harari	365	218	
	AC❖	5,583,812	12/10/96	Harari	365	185.33	
	AD❖	5,594,691	01/14/97	Bashir	365	189.09	
	AE❖	5,596,527	01/21/97	Tomioka et al.	365	185.20	
	AF❖	3,660,819	05/02/72	Frohmman-Bentchkowsky	317	235R	
Ju	AG❖	5,295,255	03/15/94	Malecek et al.	395	425	
	AH❖						
	AI❖						
	AJ❖						
	AK❖						

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ju	AO	3,755,721	8/28/73	Frohman-Bentchkowsky	317	235R	
	AP	5,021,999	6/4/91	Kohda et al.	365	168	
	AQ	4,903,236	2/20/90	Nakayama et al.	365	185	
	AR	5,394,362	2/28/95	Banks	365	189.01	
ju	AS	5,764,571	6/9/98	Banks	365	189.01	

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ju	AS	Intel Corporation. "2764A Advanced 64K (8K x 8) Production and UV Erasable PROMs." Memory Components Handbook. (October 1985) : 4.10-4.20.					
	AT	Alberts, G.S., and Kotecha, H.N. "Multi-Bit Storage FET EAROM Cell." IBM Technical Disclosure Bulletin, Vol. 24, No. 7A. (December 1981) : 3311-3314.					
	AU	Blyth, Trevor, et al. "TPM 11.7: A Non-Volatile Analog Storage Device Using EEPROM Technology." 1991 IEEE International Solid-State Circuits Conference, Digest of Technical Papers. (February 1991) : 192-193 and 315.					
	AV	Donoghue, Bill, et al. "A 256K HCMOS ROM Using a Four-State Cell Approach." IEEE Journal of Solid-State Circuits, Vol. SC-20, No. 2. (April 1985) : 598-602.					
ju	AW	"Mid-Level Current Generator Circuit", IBM Technical Disclosure Bulletin, Vol. 33, No. 1B, 1 June 1990, pp. 386-388					

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Gu	AA	5,200,920	04/06/93	Norman et al.	365	185	
Gu	AB	Re 32,401	04/14/87	Belistein, Jr. et al	365	182	
	AC						
	AD						
	AE						
	AF						
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	AI						
	AJ						
	AK						

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Examiner Initial		Document Number	Date	Country	Class	Sub-class	Translation
Gu	AL	56-114199	09/08/81	Japan	—	—	No
	AM	61-239497	10/24/86	Japan	—	—	No
	AN	61-239498	10/24/86	Japan	—	—	No
	AO	62-24499	02/02/87	Japan	—	—	No
Gu	AP	1-159895	06/22/89	Japan	—	—	No
	AQ						

OTHER PUBLICATIONS, BOOKS, PERIODICALS, AND OTHER DOCUMENTS

Gu	AR	Torelli, Guido et al., "An Improved Method for Programming a Word-Erasable EEPROM", <u>Alta Frequenza - Scientific Review in Electronics</u> , Vol. LII, No. 6, Pages 487-494 (1983).					
Se	AS	Yoshikawa, Kuniyoshi et al., "An Asymmetrical Lightly-Doped Source (ALDS) Cell for Virtual Ground High Density EPROMs", <u>IEEE International Electron Devices Meeting</u> , 1988, Pages 432-435.					

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Gu	AA	4,809,224	02/28/89	Suzuki et al.	365	168	
	AB	5,872,735	02/16/99	Banks	365	189.01	
	AC	6,002,614	12/14/99	Banks	365	189.01	
	AD	6,104,640	08/15/00	Banks	365	189.01	
	AE	6,011,716	01/04/00	Banks	365	185.03	
	AF	6,014,327	01/11/00	Banks	365	185.03	
	AG	6,118,692	09/12/00	Banks	365	185.03	
	AH	6,246,613	06/12/01	Banks	365	189.01	
	AI	6,243,321	06/05/01	Banks	365	233	
	AJ	6,343,034	01/29/02	Banks	365	189.00	
	AK	6,356,486	03/12/02	Banks	365	189.01	
	AL	6,353,554	03/05/02	Banks	365	185.03	
	AM	6,339,545	01/15/02	Banks	365	185.03	
	AN	6,324,121	11/27/01	Banks	365	185.03	
	AO	6,327,189	12/04/01	Banks	365	189.01	
	AP	6,404,675	06/11/02	Banks	365	185.03	
	AQ	6,344,998	02/05/02	Banks	365	185.22	
	AR	6,434,050	08/13/02	Banks	365	185.2	
	AS	6,381,172	04/30/02	Banks	365	185.03	
Gu	AT	2003/0202378	10/30/03	Banks	365	185.03	
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